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Lawrence J Merkel
Conley Rose & Tayon PC
P O Box 398
Austin, TX 78767-0398

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

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Office Action Summary	Application No.	Applicant(s)	
	09/483,101	MCGRATH ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 November 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-22 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Drawings as received on 13 November 2002; IDS as received on 13 November 2002; and Amendment A as received on 13 November 2002.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

5. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over copending Application No. 09/483,636 (herein referred to as copending application) in view of James L. Turley's Advanced 80386 Programming Techniques © 1988 (herein referred to as Turley).

7. Referring to claim 1, the copending application has taught a processor comprising

   a. A segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication (copending application claim 1)

b. A control register configured to store an enable indication (copending application claim 1)

c. Wherein said processor is configured to establish an operating mode responsive to said enable indication and said first operating mode indication (copending application claim 1)

8. In regards to the copending application, it is generally accepted in the art that operating mode refers to the operand size and address size, which applies to both physical and virtual addresses, and it does not matter what size the operand and address sizes are. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955) (herein referred to as *In re Rose*).

9. Copending application has not taught a segment descriptor including second operating mode indication and wherein said processor is configured to establish an operating mode responsive to said second operating mode indication. Turley has taught a processor comprising a second operating mode indication and wherein said processor is configured to establish an operating mode responsive to said second operating mode indication (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table). It would have been obvious to a person of ordinary skill in the art to incorporate Turley's second operating mode indication and response to it, because the second operating mode indicator allows for more than two combinations and/or choices of modes to be made. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the second operating mode, as taught by Turley, in the segment descriptor of copending application to allow more choices mode choices to be made.

10. Referring to claim 2, copending application has taught a processor wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in a first state (copending application claim 1). Copending application has not taught a processor wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state. Turley has taught wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1). It would have been obvious to a person of ordinary skill in the art to select an operating mode as taught by Turley, <u>because</u> it would allow the processor to select which architecture to use. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to choose a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state to select architectures.

11. Referring to claim 3, copending application has not taught a processor wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state or said second operating mode indication. Turley has taught a processor wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said

one of said plurality of operating modes is selected in response to a state or said second operating mode indication (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1). It would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a processor as taught by Turley, because it allows for more operating modes to be chosen from. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the plurality of mode in the processor of Turley in the invention of copending application to allow more operating mode choices.

12. Referring to claim 4, copending application does not teach one of said plurality of operating modes is a 32 bit operating mode. Turley has taught one of said plurality of operating modes is a 32 bit operating mode (Turley pages 53-54, Paragraphs 3 to 1). It would have been obvious to a person of ordinary skill in the art to incorporate a 32 bit operating mode of Turley, because it would allow for compatibility with extraneous systems running in a 32 bit operating mode. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the 32 bit operating mode of Turley in the device of copending application for compatibility.

13. Referring to claim 5, copending application does not teach one of said plurality of operating modes is a 16 bit operating mode. Turley does teach one of said plurality of operating modes is a 16 bit operating mode (Turley Page 53-54, Paragraphs 3 to 1). It would have been obvious to a person of ordinary skill in the art to incorporate the 16 bit operating mode as taught by Turley, because it allows the processor to be compatible with programs made for the 8086 architecture and other legacy architecture running on a 16 bit operating mode. Therefore, it

would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the 16 bit operating mode, as taught by Turley, in the invention of copending application to allow for backwards compatibility.

14. Referring to claim 6, copending application has taught said first operating mode includes a default address size, which is greater than 32 bits (copending application claim 1).

15. Referring to claim 7, copending application has taught said default address size applies to virtual addresses generated by said processor (copending application claims 1).

16. Referring to claim 8, copending application has not taught explicitly wherein a virtual address is generated according to a segmentation mechanism employed by said processor. Turley has taught wherein a virtual address is generated according to a segmentation mechanism employed by said processor (Turley Pages 160-161). It would have been obvious to a person of ordinary skill in the art to incorporate Turley's segmentation mechanism, because segmentation allows sizes to be intermixed freely. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the segmentation mechanism of Turley in the device of copending application.

17. Referring to claim 9, copending application has taught wherein said default address size further applies to physical addresses generated by said processor (copending application claim 4).

18. Referring to claim 10, copending application has not taught a processor wherein if said enable indication is in a disabled state, said first operating mode indication is undefined and said processor is configured to establish said operating mode responsive to said second operating mode indication. Turley has taught a processor wherein if said enable indication is in a disabled

state, said first operating mode indication is undefined (Turley page 26, element Control Register 0, PE and Pages 51-52). It would have been obvious to a person of ordinary skill in the art to incorporate the processor details above, as taught by Turley, because if the processor were to be compatible with older programs and systems, the flag being used to indicate the first operating mode would be undefined in the older systems. Therefore it would have been obvious to incorporate the details of a processor, which, if the enable indication is in a disabled state, the first operating mode indication is undefined to allow for backwards compatibility.

19. Referring to claim 11, copending application has taught:

a. A control register configured to store an enable indication (copending application claim 1)

b. Wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state (copending application claims 1)

20. In regards to the copending application, it is generally accepted in the art that operating mode refers to the operand size and address size, which applies to both physical and virtual addresses, and it does not matter what size the operand and address sizes are. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955) (herein referred to as *In re Rose*).

21. Copending application has not taught a segment register configured to store a segment selector and information from a segment descriptor, wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled, said segment descriptor stored in said segment descriptor table in an entry indicated by said index,

wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector, said segment descriptor including an operating mode indication. A segment register configured to store a segment selector (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4) and information from a segment descriptor (Turley Page 63, Paragraph 4), wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled (Turley Page 63, Paragraphs 4-5), said segment descriptor stored in said segment descriptor table in an entry indicated by said index (Turley Page 63, Paragraphs 4-5), wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector (Turley Page 63, INDEX), said segment descriptor including an operating mode indication (Turley Page 51-52). It would have been obvious to a person of ordinary skill in the art to incorporate the above by Turley, because this segmentation technique allows for variable byte sizes and external programs based on previous processors that used segmentation, such as the Intel 80386 and Pentium®, would require segmentation to function properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the segmentation register, selector, descriptor, and tables above, as taught by Turley, in the invention of copending application for flexibility and backwards compatibility. In regards to the copending application, it is generally accepted that setting the operating mode establishes the size of the operand, and the exact operand size does not matter. See *In re Rose*.

22. Referring to claim 12, copending application has taught wherein physical addresses are greater than 32 bits in said operating mode (copending application claim 4).

23. Referring to claim 13, copending application has taught wherein physical addresses are a first number of bits less than or equal to 64 bits (copending application claim 5).

24. Referring to claim 14, copending application has taught wherein virtual addresses are a first number less than or equal to 64 bits (copending application claim 3).

25. Referring to claim 15, copending application has not taught wherein said segment descriptor further includes a privilege level. Turley has taught a segment descriptor includes a privilege level (Turley page 51, element DPL). It would have been obvious to a person of ordinary skill in the art to incorporate the privilege level in the segment descriptor, as taught by Turley, because it controls access to the segment. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a segment descriptor which includes a privilege level, as taught by Turley, in the invention of copending application to control access to the segment.

26. Referring to claim 16, copending application has not taught a processor further comprising a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state. Turley has taught multiple control registers which allow modification of the state of the processor (Turley page 10, element Memory Segmentation). It would have been obvious to a person of ordinary skill in the art to include another indication in a control register separate from the enable to signal when a segment descriptor will be read, because it allows the user to control the state of the segmentation unit in the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a second control

register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state, as taught by Turley, in the invention of copending application to increase control over segmentation.

27. Referring to claim 17, copending application has taught a method:

a. Establishing an operating mode in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor (copending application claim 9)

b. Fetching operands (copending application claim 21) and generating addresses in response to said operating mode (copending application claim 9)

28. In regards to the copending application, it is generally accepted in the art that operating mode refers to the operand size and address size, which applies to both physical and virtual addresses, and it does not matter what size the operand and address sizes are. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955) (herein referred to as *In re Rose*).

29. Copending application has not taught a second operating mode indication in said segment descriptor. Turley has taught a processor comprising a second operating mode indication (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table). It would have been obvious to a person of ordinary skill in the art to incorporate Turley's second operating mode indication, <u>because</u> the second operating mode indicator allows for more than two combinations and/or choices of modes to be made. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the second operating mode, as taught by

Turley, in the segment descriptor of copending application to allow more choices mode choices to be made.

30. Referring to claim 18, copending application has taught a method wherein said establishing comprises establishing a first operating mode responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first operating mode includes a default address size greater than 32 bits (copending application claim 9). In regards to the copending application, it is generally accepted in the art that operating mode refers to the operand size and address size, and it does not matter what size the operand and address sizes are. See *In re Rose*.

31. Referring to claim 19, copending application has taught a method wherein said default address size applies to a virtual address (copending application claim 9).

32. Referring to claim 20, copending application has taught a method wherein said default address size applies to a physical address (copending application claim 11).

33. Referring to claim 21, copending application has not taught a method wherein said establishing further comprises establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode indication being in said first state, and wherein said second operating mode includes a default address size of 32 bits. Turley has taught establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode being in said first state, and wherein said second operating mode includes a default address size of 32 bits (Turley Page 51-52; Page 50, Figure 2-3; Page 51, element D Bit; Pages 53-54, Paragraphs 3 to

1; and Page 55, Paragraph 1). It would have been obvious to a person of ordinary skill in the art to establish a second operating mode as taught by Turley, because it would allow the processor to run multiple different types of instruction and address architectures. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to establish a second operating mode as taught by Turley in the invention of copending application to increase compatibility with other architectures.

34. Referring to claim 22, copending application has not taught establishing one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication. Turley has taught establishing one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1). It would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate a processor as taught by Turley, because it allows for more operating modes to be chosen from. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the plurality of mode in the processor of Turley in the invention of copending application to allow more operating mode choices.

35. These are provisional obviousness-type double patenting rejections.

Claim Rejections - 35 USC § 102

36. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

37. Claims 1-5, 10 and 17 are rejected under 35 U.S.C. 102(b) as being taught by James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley).

38. Referring to claim 1, Turley has taught a processor comprising:

a. A segment register configured to store a segment selector (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4) identifying a segment descriptor (Turley Page 63, Paragraph 4) including a first operating mode indication and a second operating mode indication (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table)

b. A control register configured to store an enable indication (Turley Page 26, Control Register 0, element PE)

c. Wherein said processor is configured to establish an operating mode responsive to said enable indication, said first operating mode indication, and said second operating mode indication (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3).

39. Referring to claim 2, Turley has taught wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in

a first state, and wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1).

40. Referring to claim 3, Turley has taught wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1).

41. Referring to claims 4 and 5, Turley has taught wherein one of said plurality of operating modes is a 32 bit operating mode (Applicant Claim 4) and wherein one of said plurality of operating modes is a 16 bit operating mode (Applicant Claim 5) (Turley Page 53-54, Paragraphs 3 to 1).

42. Referring to claim 10, Turley has taught wherein, if said enable indication is in a disabled state, said first operating mode indication is undefined and said processor is configured to establish said operating mode responsive to said second operating mode indication (Turley Page 26, Control Register 0, element PE and Page 51-52).

43. Referring to claim 17, Turley has taught a method comprising:

   a. Establishing an operating mode in a processor (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3) in response an enable indication in a control register within said processor (Turley Page 176, Paragraph 1 and Page 178, Paragraph 2-

3), a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table)

b. Fetching operands and generating addresses in response to said operating mode (Turley Page 52, Paragraph 2).

Claim Rejections - 35 USC § 103

44. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

45. Claims 6-9, 11-16, and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's <u>Advanced 80386 Programming Techniques</u> (herein referred to as Turley) in view of Khalidi et al., U.S. Patent Number 5,479,627 (herein referred to as Khalidi).

46. Referring to claim 6, Turley has not explicitly taught wherein said first operating mode includes a default address size, which is greater than 32 bits. However, Turley has taught a first operating mode with a default address size, which is equal to 32, bits (Turley Pages 51-52 and Pages 53-54, Paragraphs 3 to 1). Khalidi has an address size, which is greater than 32 bits (Khalidi column 6, lines 25-57). It would have been obvious to a person of ordinary skill in the art to incorporate the address size, which is greater than 32 bits of Khalidi, <u>because</u> the larger address size would allow for more address locations to be referenced. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to

incorporate the larger address size of Khalidi in the first operating mode of Turley to increase the addressable area of the device. Also, the size of the address does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

47. Referring to claim 7, Turley has taught wherein said default address size applies to virtual addresses generated by said processor (Turley Page 11, Paging and Page 47, Paragraph 3).

48. Referring to claim 8, Turley has taught wherein a virtual address is generated according to a segmentation mechanism employed by said processor (Turley Page 47, Paragraph 3 and Page 160-162).

49. Referring to claim 9, Turley has taught wherein said default address size further applied to physical addresses generated by said processor (Turley Page 46, Paragraphs 2-3 and Page 456, Physical Address).

50. Referring to claim 11, Turley has taught a processor comprising:

a. A segment register configured to store a segment selector (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4) and information from a segment descriptor (Turley Page 63, Paragraph 4), wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled (Turley Page 63, Paragraphs 4-5), said segment descriptor stored in said segment descriptor table in an entry indicated by said index (Turley Page 63, Paragraphs 4-5), wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector (Turley Page 63, INDEX), said segment descriptor including an operating mode indication (Turley Page 51-52)

b. A control register configured to store an enable indication (Turley Page 26, Control Register 0, element PE).

51. Turley has not explicitly taught wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state. However, Turley has taught an operating mode responsive to said enable indication being in an enabled state (Turley Page 26, Control Register 0, element PE) and said operating mode indication being in a first state (Turley Pages 51-52). Khalidi has taught virtual addresses are greater than 32 bits (Khalidi column 6, lines 25-27). It would have been obvious to a person of ordinary skill in the art to incorporate the address size, which is greater than 32 bits of Khalidi, because the larger address size would allow for more address locations to be referenced. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the larger address size of Khalidi in the first operating mode of Turley to increase the addressable area of the device. Also, the size of the address does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

52. Referring to claim 12, Turley has not taught wherein physical addresses are greater than 32 bit in said operating mode. Khalidi has taught wherein physical addresses are greater than 32 bit in said operating mode (Khalidi column 6, lines 25-27). It would have been obvious to a person of ordinary skill in the art to incorporate the address size, which is greater than 32 bits of Khalidi, because the larger address size would allow for more address locations to be referenced. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the larger address size of Khalidi in the first operating mode

of Turley to increase the addressable area of the device. Also, the size of the address does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

53. Referring to claims 13 and 14 Turley has not taught wherein physical (Applicant Claim 13) and virtual (Applicant Claim 14) addresses are a first number of bits less than or equal to 64 bits. Khalidi has taught wherein physical and virtual addresses are a first number of bits less than or equal to 64 bits (Khalidi column 6, lines 25-27). It would have been obvious to a person of ordinary skill in the art to limit the physical and virtual addresses to less than or equal to 64 bits as taught by Khalidi, because by limiting the size to 64 bits, the device adheres to the IEEE standard followed by most users. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the size of Khalidi in the device of Turley to ensure compatibility with standards. Also, the size of the address does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

54. Referring to claim 15, Turley has taught wherein said segment descriptor further includes a privilege level (Turley Page 51, DPL).

55. Referring to claim 16, Turley has taught the processor further comprising a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state (Turley Page 10, Memory Segmentation).

56. Referring to claim 18, Turley has taught wherein said establishing comprises establishing a first operating mode responsive to said enable indication is in an enabled state and said first operating mode indication is in a first state (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1). Turley has not explicitly taught wherein said

first operating mode includes a default address size greater than 32 bits. However, Turley has taught said operating mode includes a default address size (Turley Page 51, D Bit). Khalidi has taught virtual addresses are greater than 32 bits (Khalidi column 6, lines 25-27). It would have been obvious to a person of ordinary skill in the art to incorporate the address size, which is greater than 32 bits of Khalidi, <u>because</u> the larger address size would allow for more address locations to be referenced. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the larger address size of Khalidi in the first operating mode of Turley to increase the addressable area of the device. Also, the size of the address does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

57. Referring to claim 19, Turley has taught wherein said default address size applies to a virtual addresses (Turley Page 11, Paging and Page 47, Paragraph 3).

58. Referring to claim 20, Turley has taught wherein said default address size further applied to a physical addresses (Turley Page 46, Paragraphs 2-3 and Page 456, Physical Address).

59. Referring to claim 21, Turley has taught wherein said establishing further comprises establishing a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication being in said first state (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1) and wherein said second operating mode includes a default address size of 32 bits (Turley Page 51, D Bit).

60. Referring to claim 22, Turley has taught wherein said establishing further comprises establishing one of a plurality of operating modes if said enable indication is in said enabled state

and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Turley Page 51-52; Page 50, Figure 2-3; Pages 53-54, Paragraphs 3 to 1; and Page 55, Paragraph 1).

61. Claims 1-7, 10, 11, 14, 15, 17-19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Intel.

62. Referring to claim 1, Hammond has taught a control register configured to store an enable indication, wherein said processor is configured to establish an operating mode responsive to said enable indication, said first operating mode indication, and said second operating mode indication (Hammond columns 6-7, lines 61-9 and column 7, lines 34-39). Hammond has not taught a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication. However, Hammond does teach including a segmentation unit (Hammond column 4, lines 54-57) compatible with the x86 structure and a second operating mode indication stored in the control register (Hammond column 6-7, lines 61-9 and column 7, lines 34-39). Intel, which is based on the x86 structure and instruction set (Intel page 2-1, paragraphs 1-2), has taught that it is common to have a segment register configured to store a segment selector identifying a segment descriptor including operating mode indication (Intel page 11-9, Figure 11-6; page 11-10, paragraph 4; page 11-12, Figure 11-8; and page 11-13, item D bit/B bit). It would have been obvious to a person of ordinary skill in the art that the segmentation unit in Hammond represented the segment register, segment selector, and segment descriptor taught by Intel and to move the operating mode indicators to the segmentation unit, <u>because</u> the segment register,

selector, and descriptor are components found in a generic x86 compatible segmentation unit and moving the operating mode indicators to the segment descriptor would allow the operating mode to automatically vary depending on which selector is active and would be an advantage over a single global mode flag, which would have to use an instruction cycle to change the flag setting before the instructions in the other operating modes could be executed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication, as taught by Intel, in the invention of Hammond for backwards compatibility and to increase speed.

63. Referring to claim 2, Hammond has taught a processor wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state (Hammond columns 6-7, lines 61-69 and column 7, lines 34-39).

64. Referring to claim 3, Hammond has taught a processor wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Hammond column 4, lines 46-48; column 6-7, lines 61-9; column 7, lines 34-39; and Figure 2).

65. Referring to claim 4, Hammond has taught a processor wherein one of said plurality of operating modes is a 32 bit operating mode (Hammond column 4, lines 60-64 and column 6, lines 52-55).

66. Referring to claim 5, Hammond has taught a processor wherein one of said plurality of operating modes is a 16 bit operating mode (Hammond column 4, lines 60-64 and column 6, lines 52-55).

67. Referring to claim 6, Hammond has taught a processor wherein said first operating mode includes a default address size, which is greater than 32 bits (Hammond column 5, 12-13 and column 6, lines 52-55).

68. Referring to claim 7, Hammond has taught a processor wherein said default address size applies to virtual addresses generated by said processor (Hammond column 5, lines 12-13 and column 6, lines 52-55).

69. Referring to claim 10, Hammond has taught a processor wherein if said enable indication is in a disabled state, said first operating mode indication is undefined (Hammond column 7, lines 12-21). Hammond has not taught a processor wherein said processor is configured to establish said operating mode responsive to said second operating mode indication. Intel has taught a processor wherein said processor is configured to establish an operating mode responsive to an operating mode indication (Intel page 11-12, Figure 11-8 and page 11-13, heading D bit/B bit). It would have been obvious to a person of ordinary skill in the art to incorporate the details of the processor above, <u>because</u> this would ensure an operating mode is always established no matter the conditions. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate in a processor a

configuration to establish an operating mode responsive to an operating mode indication to ensure an operating mode is always selected.

70. Referring to claim 11, Hammond has taught a processor:

a. a control register configured to store an enable indication (Hammond columns 6-7, lines 61-69 and column 7, lines 34-39)

b. wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state (Hammond column 5, lines 12-13; column 6, lines 52-55; columns 6-7, lines 61-9; and column 7, lines 34-39)

71. Hammond has not taught a segment register configured to store a segment selector and information from a segment descriptor, wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled, said segment descriptor stored in said segment descriptor table in an entry indicated by said index, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector, said segment descriptor including an operating mode indication. However, Hammond does teach including a segmentation unit (Hammond column 4, lines 54-57) compatible with the x86 structure. Intel, which is based on the x86 structure and instruction set (Intel page 2-1, paragraphs 1-2), has taught a segment register (Intel page 11-9, heading 11.2.1) configured to store a segment selector (Intel page 11-9, Figure 11-6) and information from a segment descriptor (Intel page 11-9, Figure 11-6), wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said

processor is coupled (Intel page 11-10, Figure 11-7and paragraph 6), said segment descriptor stored in said segment descriptor table in an entry indicated by said index (Intel page 11-10, paragraph 6), wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector (Intel page 11-9, paragraph 2), said segment descriptor including an operating mode indication (Intel page 11-12, Figure 11-8 and page 11-13, item D bit/B bit). It would have been obvious to a person of ordinary skill in the art to incorporate the above by Intel, because this is a standard segmentation technique and is based on the x86 structure, which would ensure compatibility. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made that the segmentation unit in Hammond includes a segment register configured to store a segment selector and information from a segment descriptor, wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled, said segment descriptor stored in said segment descriptor table in an entry indicated by said index, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector, said segment descriptor including an operating mode indication, as taught by Intel.

72. Referring to claim 14, Hammond has taught a processor wherein virtual addresses are a first number of bits less than or equal to 64 bits (Hammond column 5, lines 17-18).

73. Referring to claim 15, Hammond has not taught wherein said segment descriptor further includes a privilege level. Intel has taught wherein said segment descriptor further includes a privilege level (Intel 11-12, Figure 11-8 and page 11-15, paragraph 2). It would have been obvious to a person of ordinary skill in the art would have included the privilege level in said

segment descriptor, because it would control access to the segment. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said segment descriptor further includes a privilege level, as taught by Intel, in the invention of Hammond to control access to the segment.

74. Referring to claim 16, Hammond has not taught a processor further comprising a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state. Intel has taught multiple control registers which allow modification of the state of the processor (Intel page 3-8, heading Registers), including the states of the segmentation unit (Intel page 10-6, Figure 10-3). It would have been obvious to a person of ordinary skill in the art to include another indication in a control register separate from the enable to signal when a segment descriptor will be read, because it allows the user to control the state of the segmentation unit in the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state, as taught by Intel, in the invention of Hammond to increase control over segmentation.

75. Referring to claim 17, Hammond has taught a method establishing an operating mode in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor (Hammond columns 6-7, lines 61-9 and column 7, lines 34-39).

Hammond has not explicitly taught fetching operands and generating addresses in response to said operating mode. Intel has explicitly taught fetching operands and generating addresses in response to said operating mode (Intel page 11-12, Figure 11-8 and page 11-13, item D bit/B bit). It would have been obvious to fetch operands and generate addresses in response to the operating mode, because when changing operating mode, the address size and operand size changes and the new sizes are required for the device to function properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to fetch operands and generate addresses in response to said operating mode, as taught by Intel, in the invention of Hammond to ensure the processor functions properly.

76. Referring to claim 18, Hammond has taught a method wherein said establishing comprises establishing a first operating mode responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first operating mode includes a default address size greater than 32 bits (Hammond column 5, lines 12-13; column 6, lines 52-55; columns 6-7, lines 61-9; and column 7, lines 34-39).

77. Referring to claim 19, Hammond has taught a method wherein said default address size applies to a virtual address (Hammond column 5, lines 12-13 and column 6, lines 52-55).

78. Referring to claim 21, Hammond has taught a method wherein said establishing further comprises establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode indication being in said first state, and wherein said second operating mode includes a default address size of 32 bits (Hammond columns 6-7, lines 61-9; column 4, lines 60-64; and column 6, lines 52-55).

79. Referring to claim 22, Hammond has taught a method wherein said establishing further comprises establishing one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication (Hammond column 4, lines 46-49; column 6-7, lines 61-9; and Figure 2).

80. Claims 8, 9, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Intel as applied to claims 1-7 above, and further in view of Alpert.

81. Referring to claim 8, Hammond in view of Intel has not taught a virtual address is generated according to a segmentation mechanism employed by said processor. However, Hammond does teach a virtual address was generated and includes a segmentation unit. Alpert has taught virtual memory, typically, is generated using techniques such as segmentation, paging, or a combination of both (Alpert column 1, lines 27-29). It would have been obvious to a person of ordinary skill in the art to use segmentation to generate a virtual address, <u>because</u> segmentation allows for variable byte sizes and external programs based on previous processors that used segmentation, such as the Intel Pentium®, would require segmentation to function properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made that a virtual address is generated according to a segmentation mechanism employed by said processor for flexibility and backwards compatibility.

82. Referring to claim 9, Hammond in view of Intel has not taught a processor wherein said default address size further applies to physical addresses generated by said processor. Alpert has taught a physical memory size greater than 32 bits (Alpert Abstract, lines 3-6), which is the default address size. It would have been obvious to a person of ordinary skill in the art to apply

the default address size of greater than 32 bits to the physical address, as taught by Alpert, because it increases the physical memory size. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said default address size further applies to physical addresses generated by said processor, as taught by Alpert, in the invention of Hammond to increase the physical memory size.

83. Referring to claim 12, Hammond in view of Intel has not taught a processor wherein physical addresses are greater than 32 bits in said operating mode. Alpert has taught a physical memory size greater than 32 bits (Alpert Abstract, lines 3-6), which is the default address size. It would have been obvious to a person of ordinary skill in the art to apply the default address size of greater than 32 bits to the physical address, as taught by Alpert, because it increases the physical memory size. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said default address size further applies to physical addresses generated by said processor, as taught by Alpert, in the invention of Hammond to increase the physical memory size.

84. Referring to claim 13, Hammond in view of Intel has not taught wherein physical addresses are a first number of bits less than or equal to 64 bits. Alpert has taught wherein physical addresses are a first number of bits less than or equal to 64 bits (Alpert column 3, lines 14-26, 35-38, and lines 44-48 and column 4, lines 32-39). It would have been obvious to a person of ordinary skill in the art to apply physical addresses that are a first number of bits less than or equal to 64 bits, as taught by Alpert, because it increases the physical memory size but maintains compatibility with previous smaller address size architectures and the IEEE standard. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made that physical addresses are a first number of bits less than or equal to 64 bits, as taught by Alpert, in the invention of Hammond to increase the physical memory size and maintain compatibility.

85. Referring to claim 20, Hammond in view of Intel has not taught a method wherein said default address size applies to a physical address. Alpert has taught a physical memory size greater than 32 bits (Alpert Abstract, lines 3-6), which is the default address size. It would have been obvious to a person of ordinary skill in the art to apply the default address size of greater than 32 bits to the physical address, as taught by Alpert, <u>because</u> it increases the physical memory size. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that said default address size further applies to physical addresses generated by said processor, as taught by Alpert, in the invention of Hammond to increase the physical memory size.

Response to Remarks

86. Applicants' amendment filed 13 November 2002, paper number 11, have been fully considered but they are not persuasive. In addition, new grounds for rejection had been introduced.

87. In the remarks, the applicants argue in essence that "there is no teaching or suggestion in Hammond or Intel to make the proposed modification... Applicants submit that the there is no evidence that generally available knowledge in the art provides the motivation for modification described above. Thus it appears that impermissible hindsight from Applicants claimed invention is being used to make the modification" on pages 3-4. This is not found persuasive because the references do not have to specifically teach the proposed modifications nor does the

suggestion to combine prior art teaching have to be found in a specific reference. See *In re Oetiker*, 24 USPQ2d 1443 (CAFC 1992) and *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988). In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

88. Furthermore, Applicants' argue "that it is unclear that the combination of Hammond and Intel, even if modified as suggested by the Office Action, would achieve the alleged advantage over a global mode flag, which would have to use an instruction to change the flag setting before the instructions in the other operating modes could be executed" on pages 4-5. This is not found persuasive because the claim language does not refer to the number of instructions needed to change the flag setting nor the global mode flag. However, Intel does have an advantage to this, because Intel's system uses one instruction that combines loading the segment register and the segment/mode flag value instruction. Therefore, Intel would only use one instruction cycle and not require the extra instruction cycle suggested by the applicants' argument.

89. In addition, applicants' argue that "Intel teaches away from the proposed modification" on page 5. This argument is not persuasive, because combining two references does not mean combining their specific structures but what the each structure suggests and what the combining of the two structures suggests to a person of ordinary skill in the art. In this particular instance, it

is combining Intel's suggestion of using a segment selector with Hammond and what the combination of these two would suggest to a person of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981); *In re Sneed*, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983); and *In re Nievelt*, 482 F.2d 965, 179 USPQ 224, 226 (CCPA 1973).

90. In regards to applicants' argument that "the D bit/B bit controls selection between 32 bit and 16 bit addresses. This does not teach or suggest 'said segment descriptor including an operating mode indication…wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state'" on page 5-6 is not applicable. The reference relied upon for teaching an operating mode in which virtual addresses are greater than 32 bits was not Intel, but Hammond. However, the D bit/B bit from Intel may just as easily been used, because the address size in each respective mode does not matter. See *In re Rose* 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

91. In regards to the argument that "when Hammond is operating in 64-bit mode, it appears that segments are not used", on page 6, Hammond does not explicitly say that segmentation is not used, but that it is not <u>required</u>. A person of ordinary skill in the art would recognize that segmentation would still be used in Hammond for the same reason that Intel used it with the 16/32 bit modes, because segmentation allows sizes to be intermixed freely.

92. Furthermore, applicants' arguments that Hammond "does not teach or suggest 'a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor'" on page 7 is not found persuasive. The applicant is correct that

Hammond does not teach operating mode indicators in a segment descriptor, however, Hammond teaches mode indicators in the control register (Hammond column 7, lines 34-39). It does not matter whether the mode indicators are in the control register or the segment descriptor, because it still functions the same. There is only a shifting of parts from the control register to the segment register. See *In re Japiske*, 181 F.2d 1019, 1023, 86 USPQ 70, 73 (CCPA 1960).

93. In response to the applicants' request for the obviousness double patenting rejection being held in abeyance, the obviousness double patenting rejection has been withdrawn in favor of the obviousness double patenting rejection above due to amendments to the copending application.

94. In response to the applicants' argument that "the drawings illustrate the various elements which perform various embodiments of the method" on page 8, the applicants' drawings did not include a flowchart or some form of diagram showing the method claimed and there was no detailed suggestion of a method outside of the claims. However, the objection is removed in favor of newly submitted Figure 13 and the according amendment to the specification.

95. In response to the applicants' remarks regarding the Official Draftsman objection on pages 8-9, the applicants' must contact the Official Draftsman directly. The number may be found on the Official Draftsman form (Form PTO-948), which accompanied the initial Office Action.

Conclusion

96. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

97. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

98. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

January 8, 2003

Eddie Chan

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100